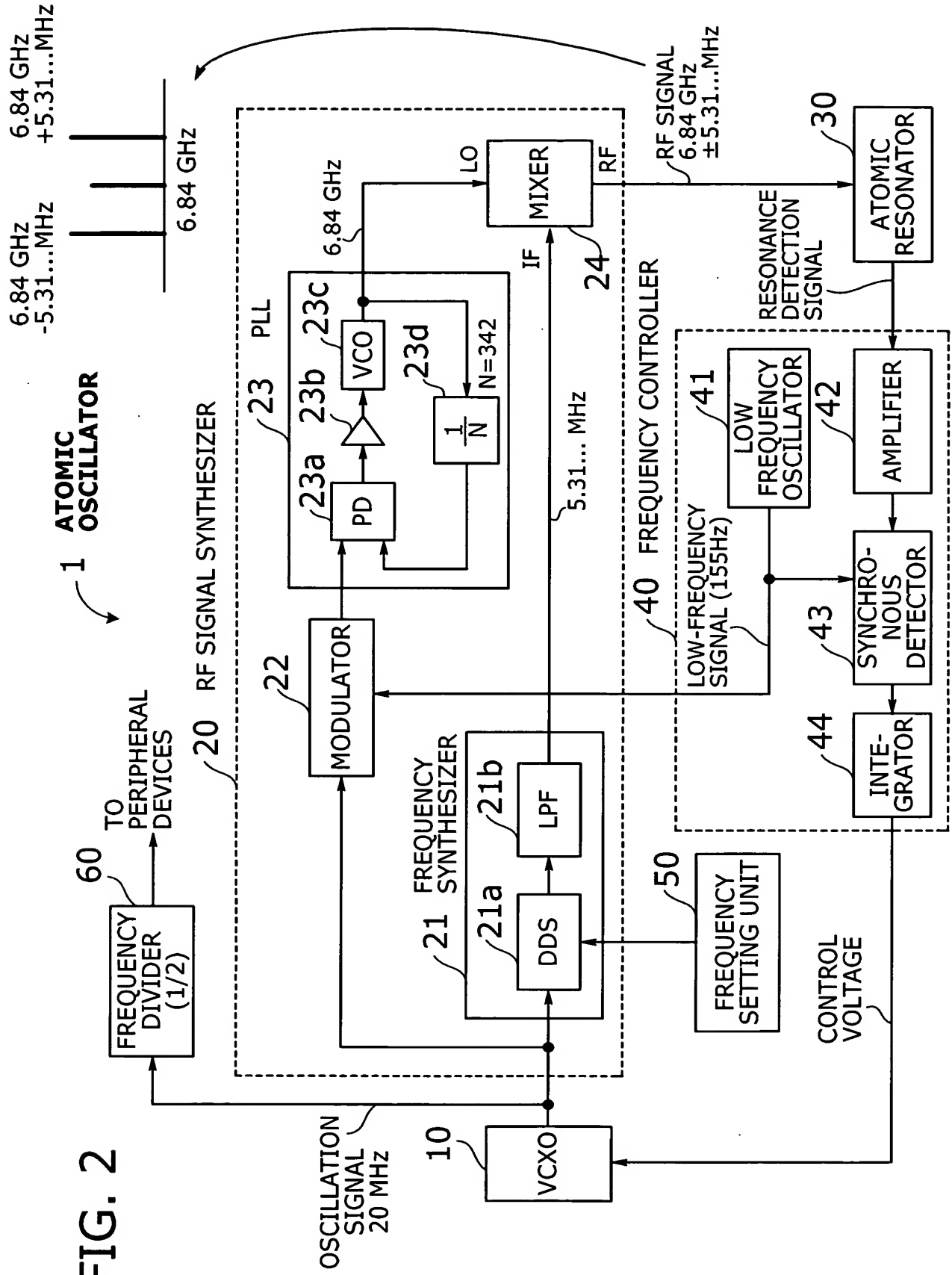


FIG. 1

FIG. 2



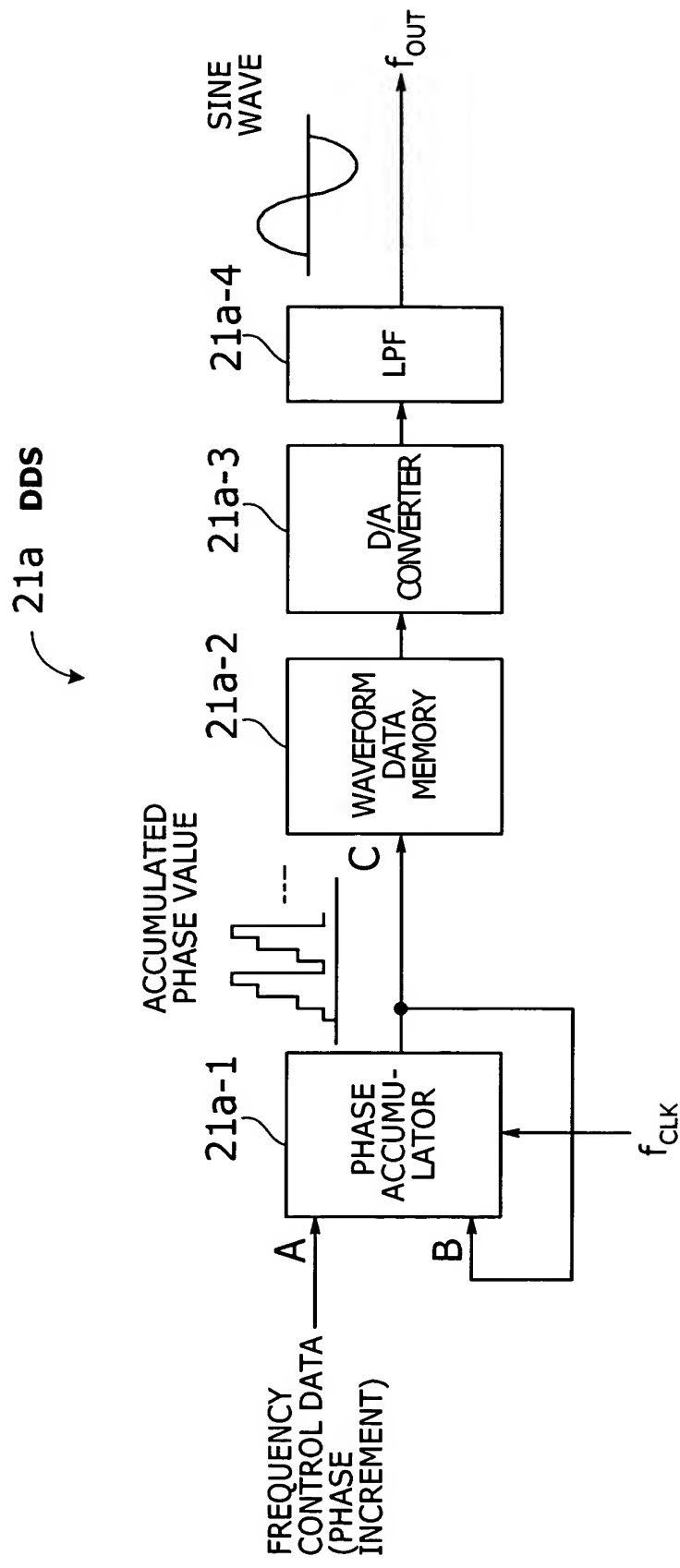


FIG. 3

T1
↙

CLOCK COUNT	ACCUMULATED PHASE OUTPUT				
	BIT #3	BIT #2	BIT #1	BIT #0	DECIMAL
0	0	0	0	0	0
1	0	0	1	1	3
2	0	1	1	0	6
3	1	0	0	1	9
4	1	1	0	0	12
5	1	1	1	1	15
6	0	0	1	0	2
7	0	1	0	1	5
8	1	0	0	0	8
9	1	0	1	1	11
10	1	1	1	0	14
11	0	0	0	1	1
12	0	1	0	0	4
13	0	1	1	1	7
14	1	0	1	0	10
15	1	1	0	1	13
16	0	0	0	0	0
17	0	0	1	1	3
18	0	1	1	0	6
19	1	0	0	1	9

FIG. 4

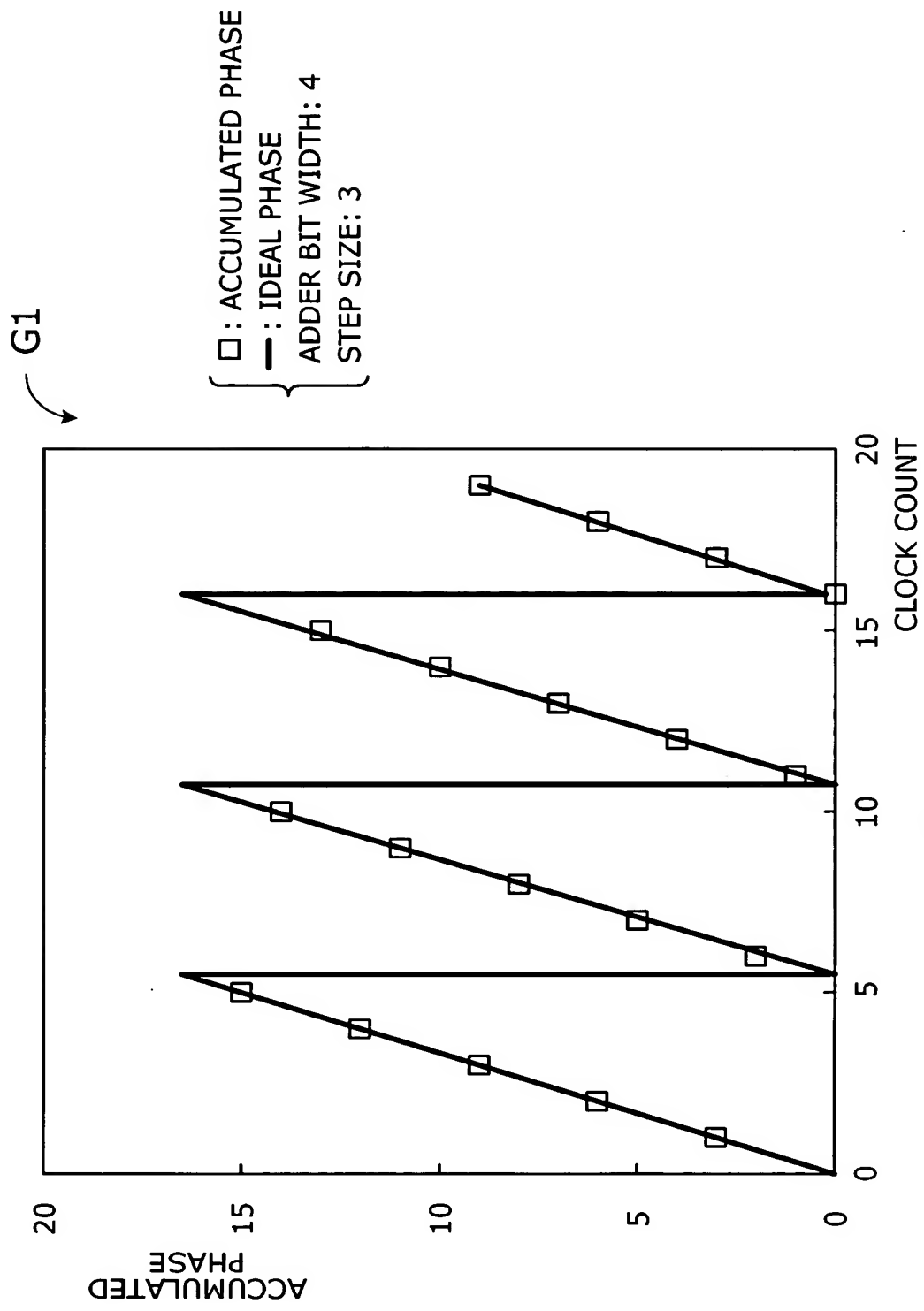
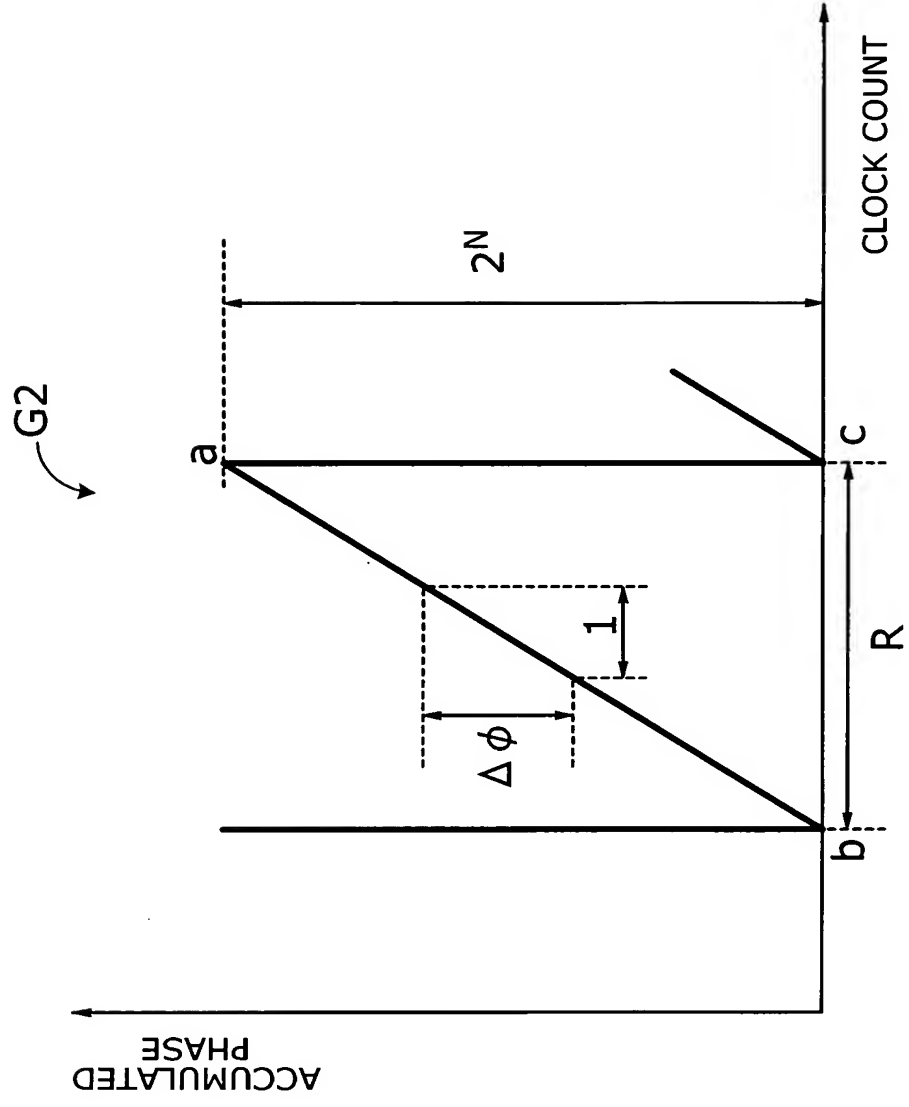


FIG. 5



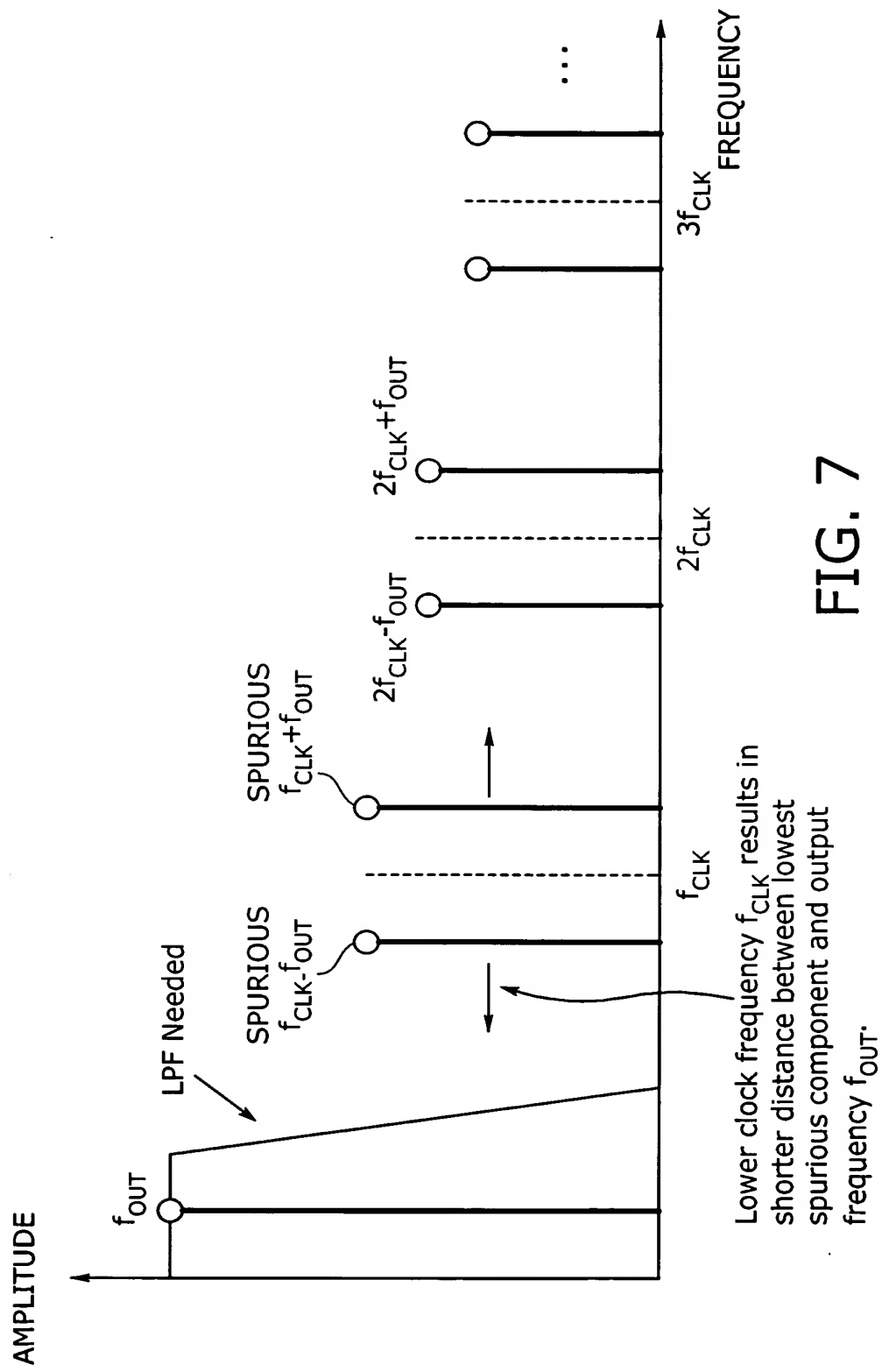


FIG. 7

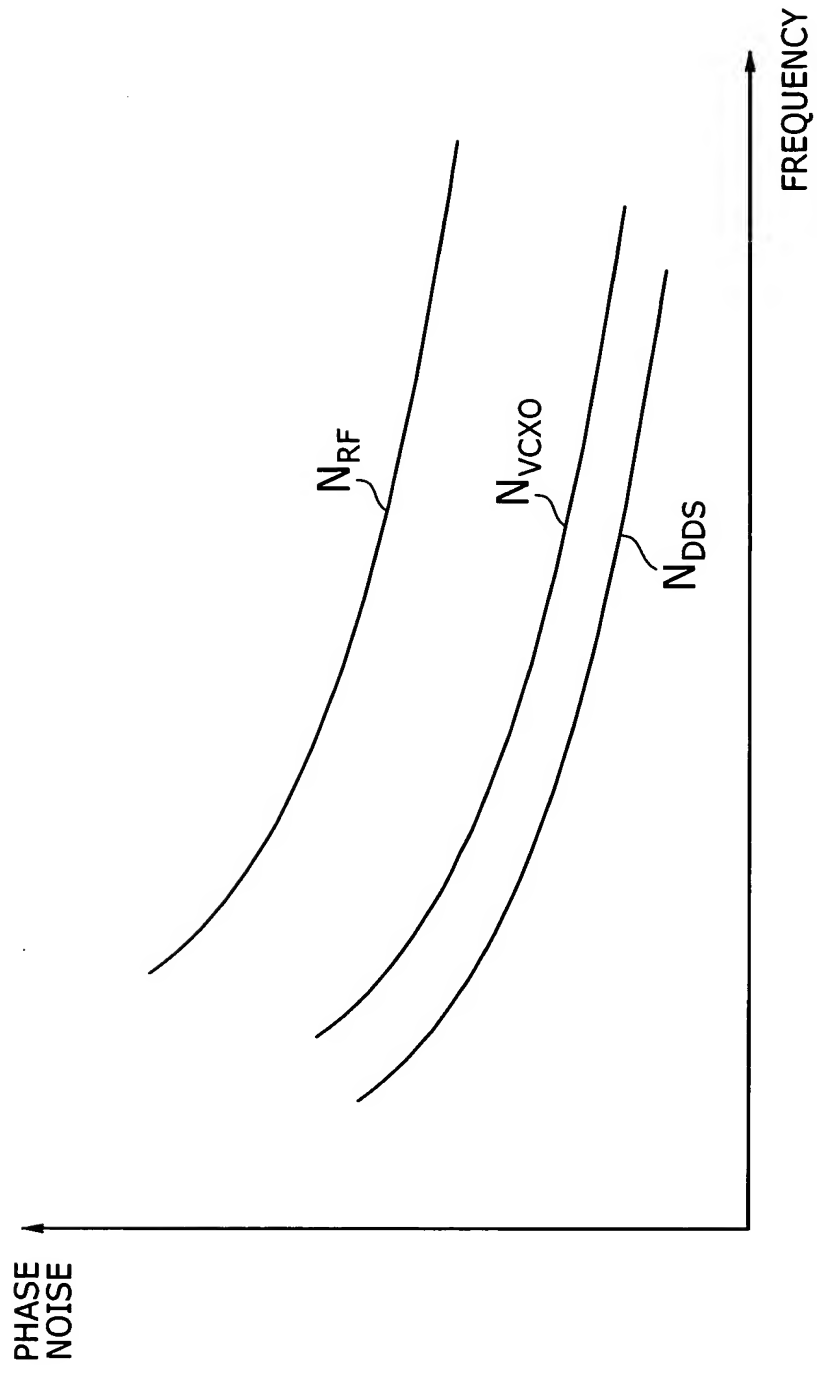


FIG. 8
PRIOR ART

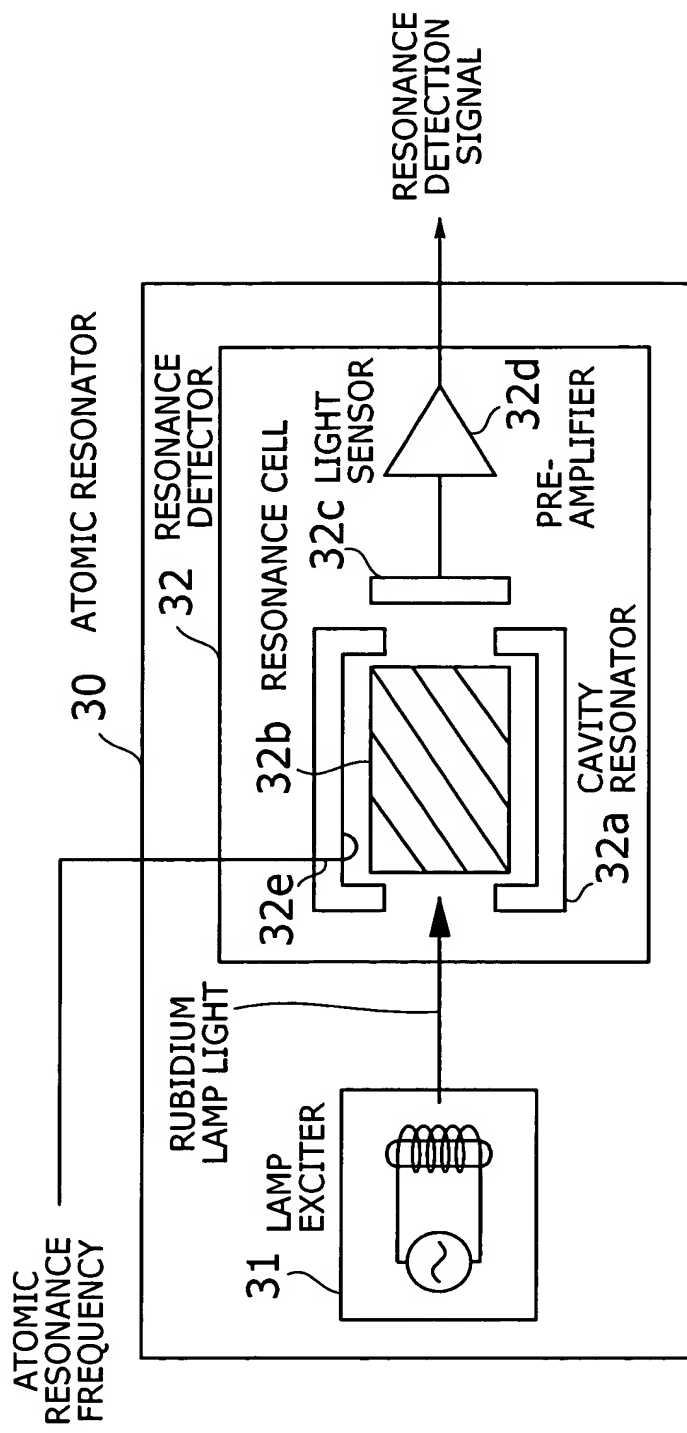


FIG. 9

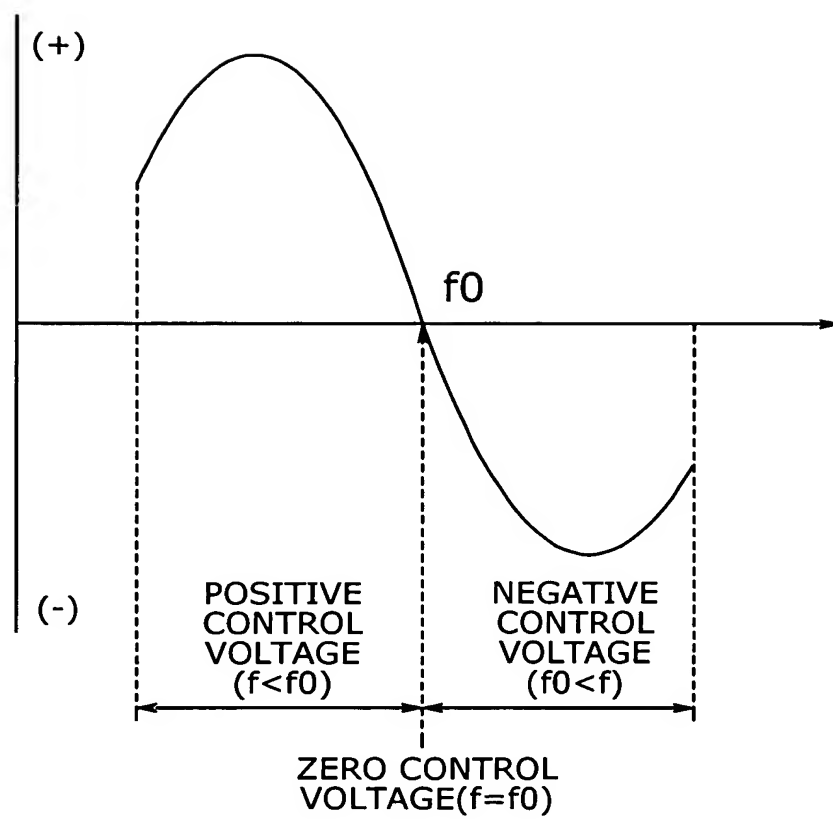
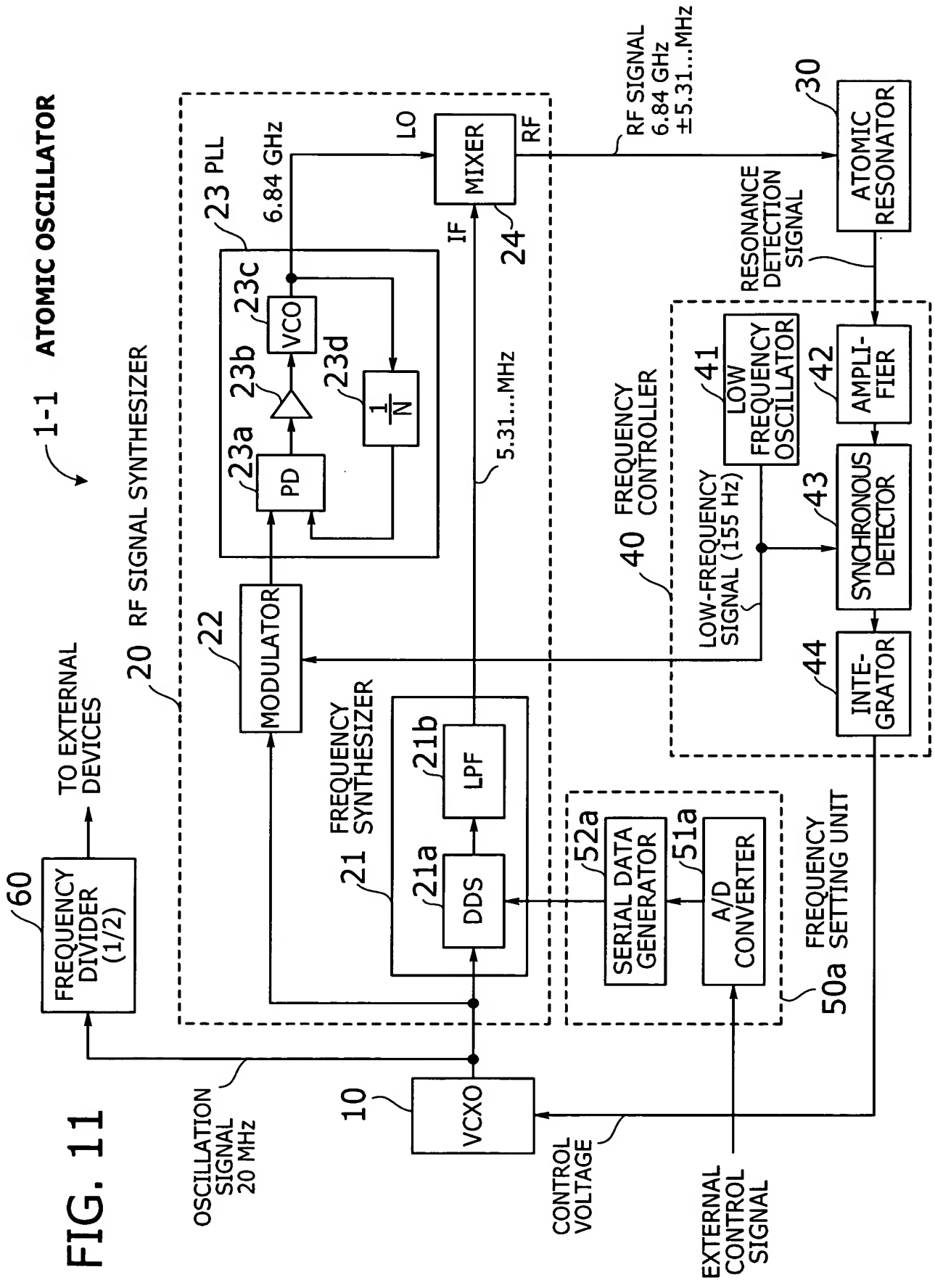
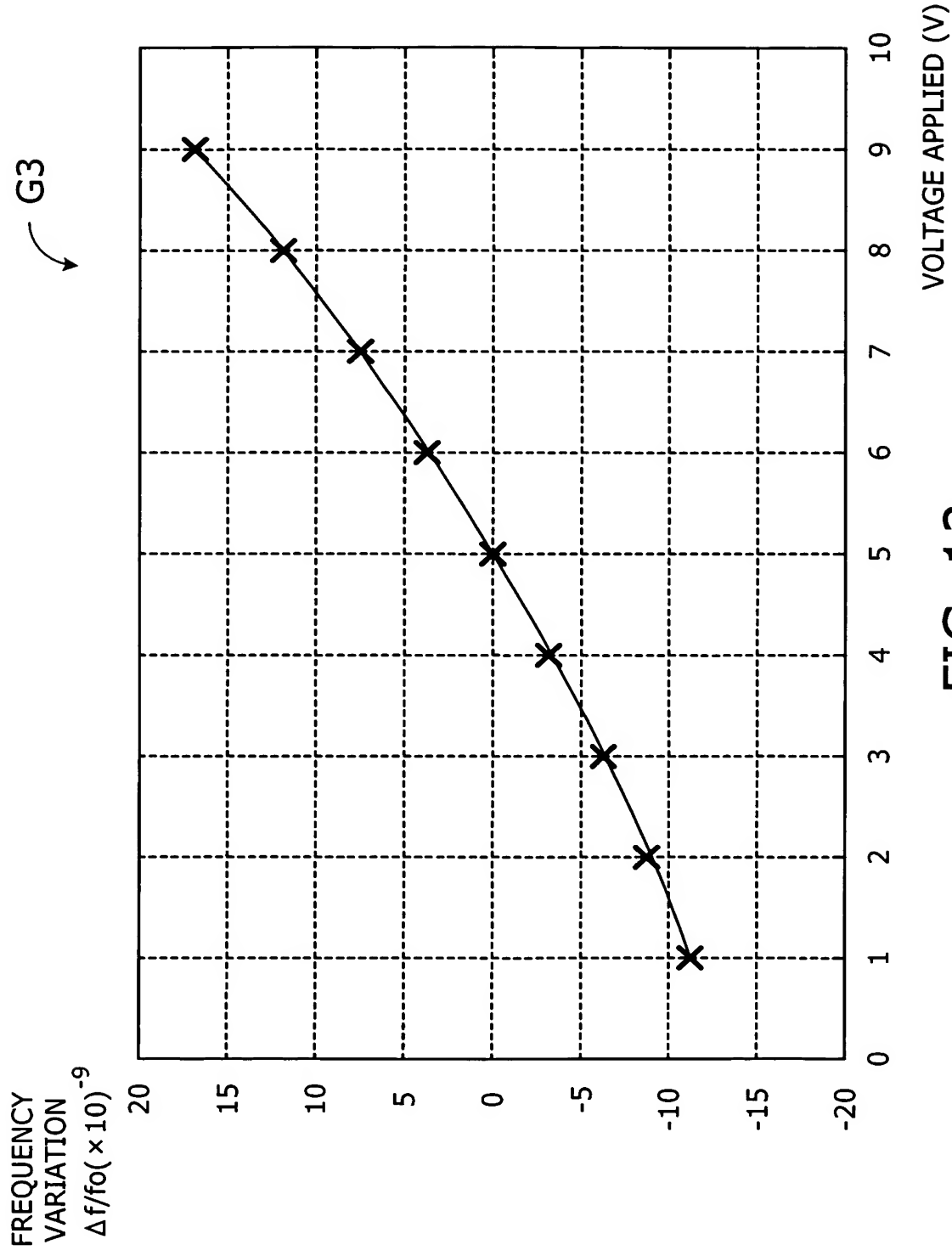


FIG. 10





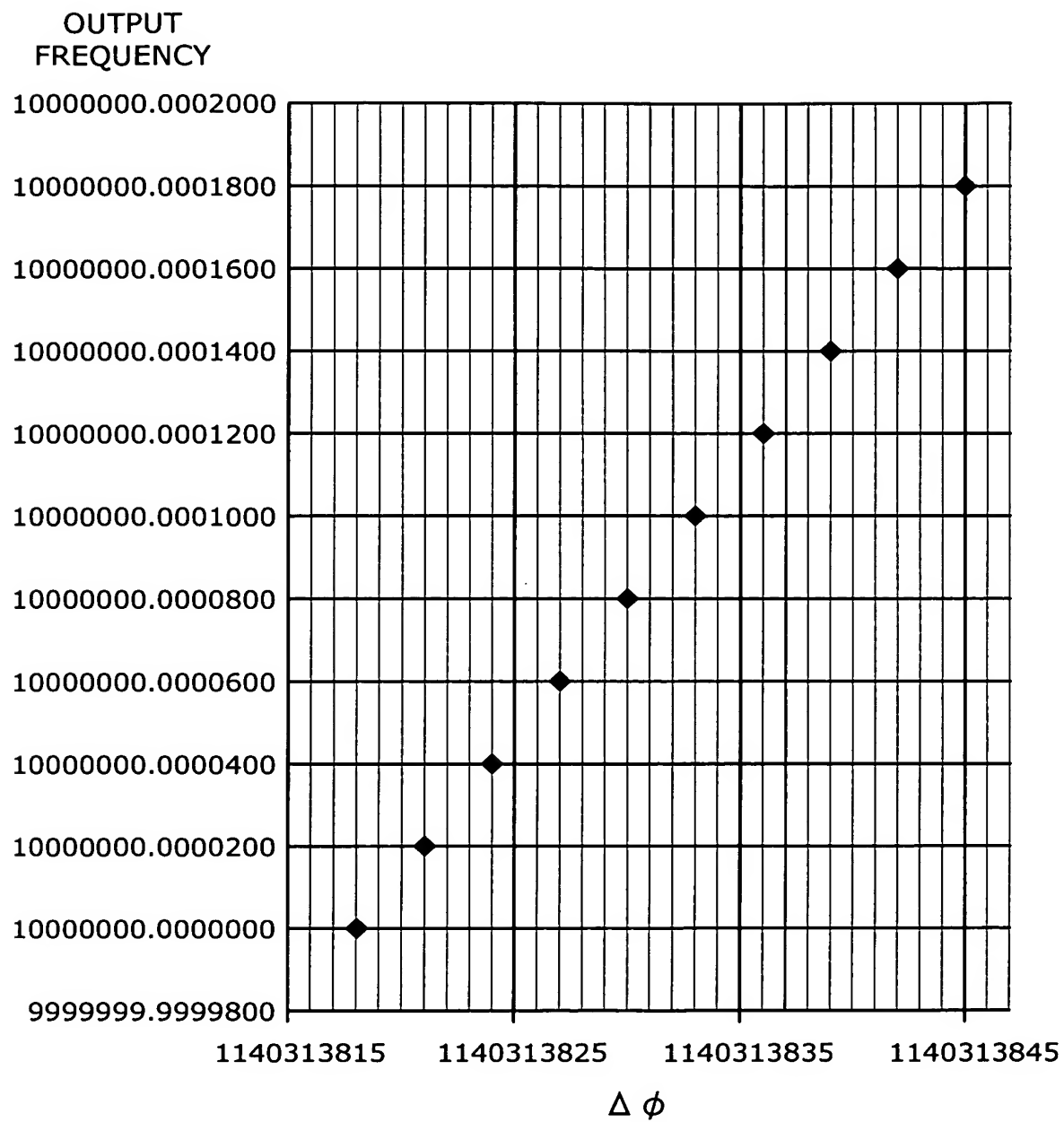


FIG. 13

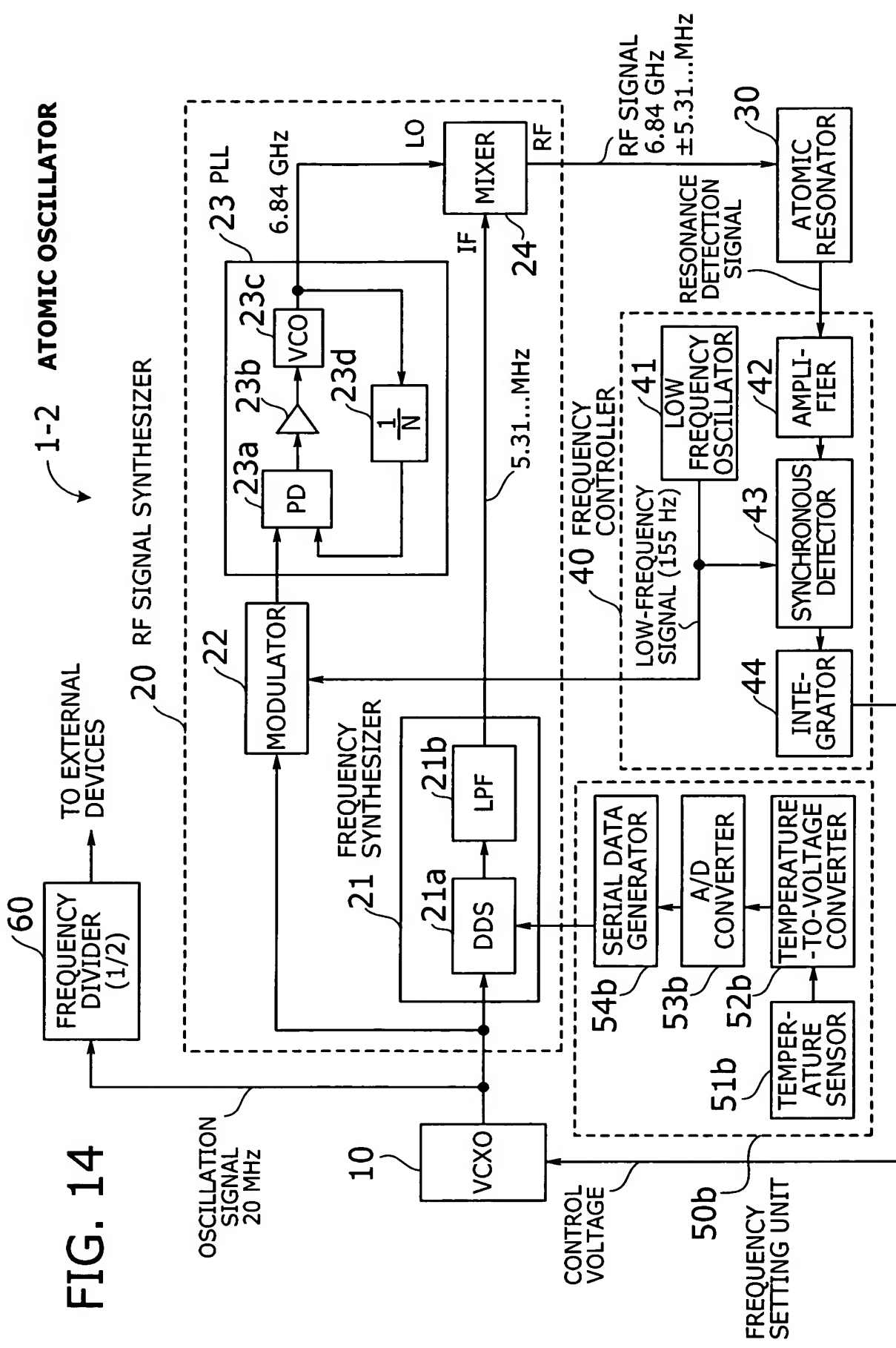
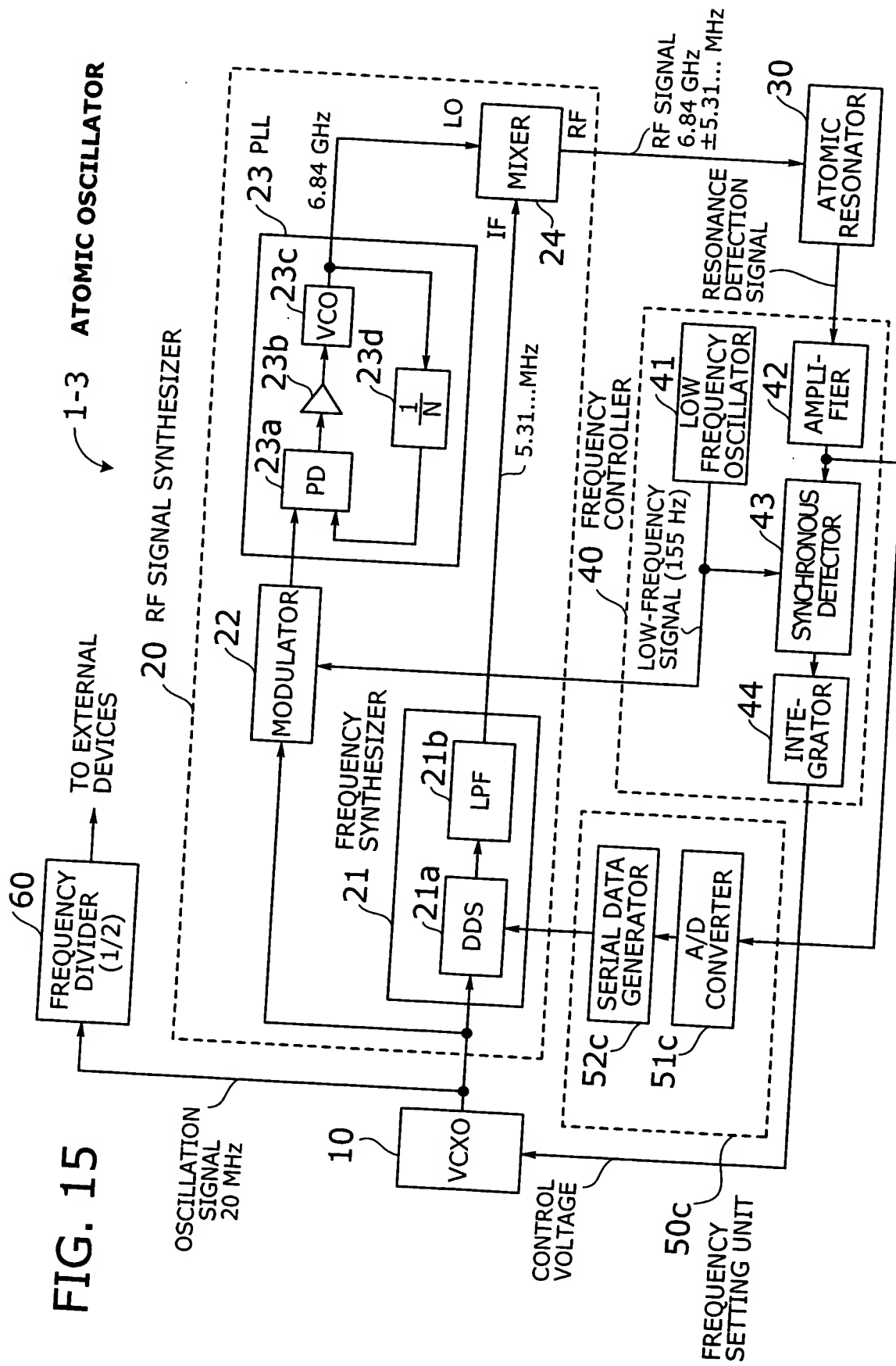


FIG. 15



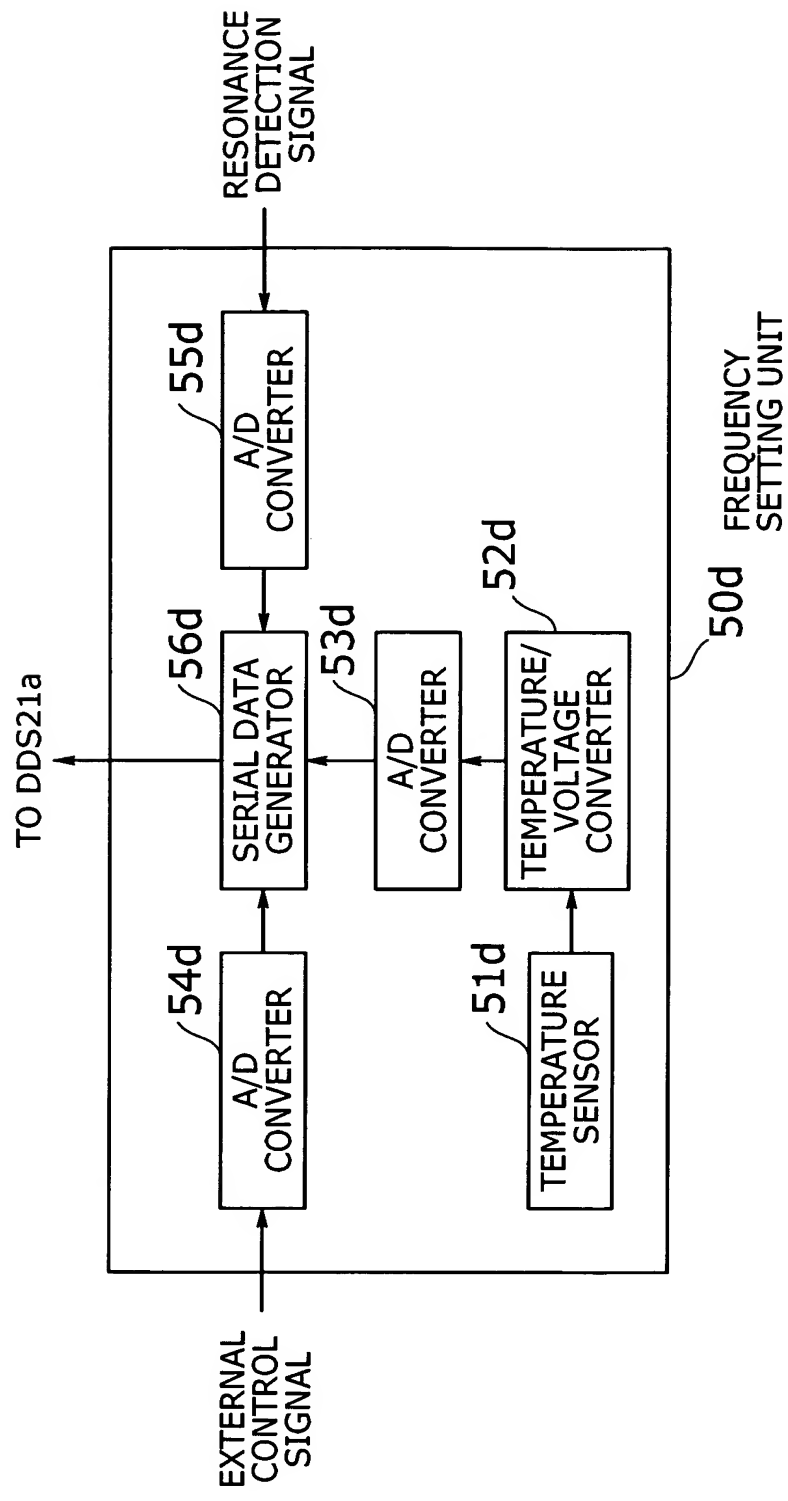
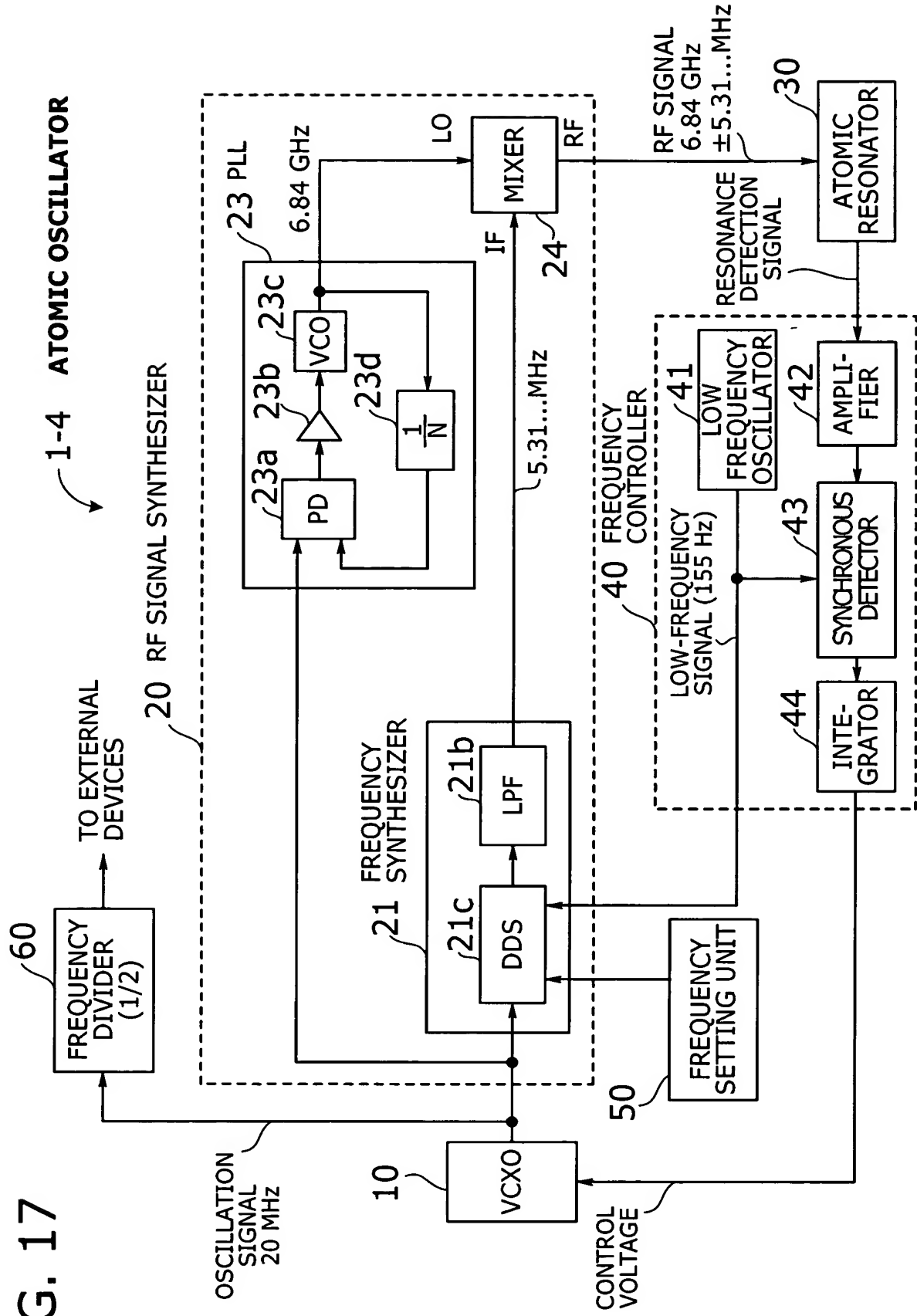


FIG. 16

FIG. 17



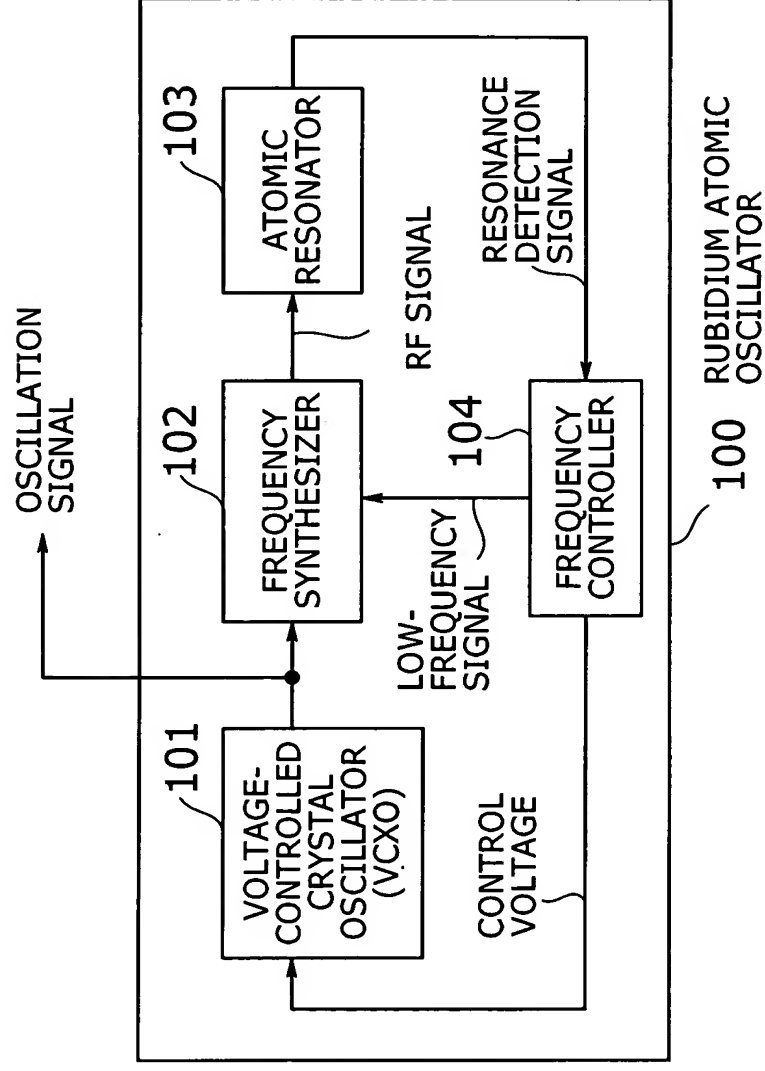


FIG. 18

PRIOR ART

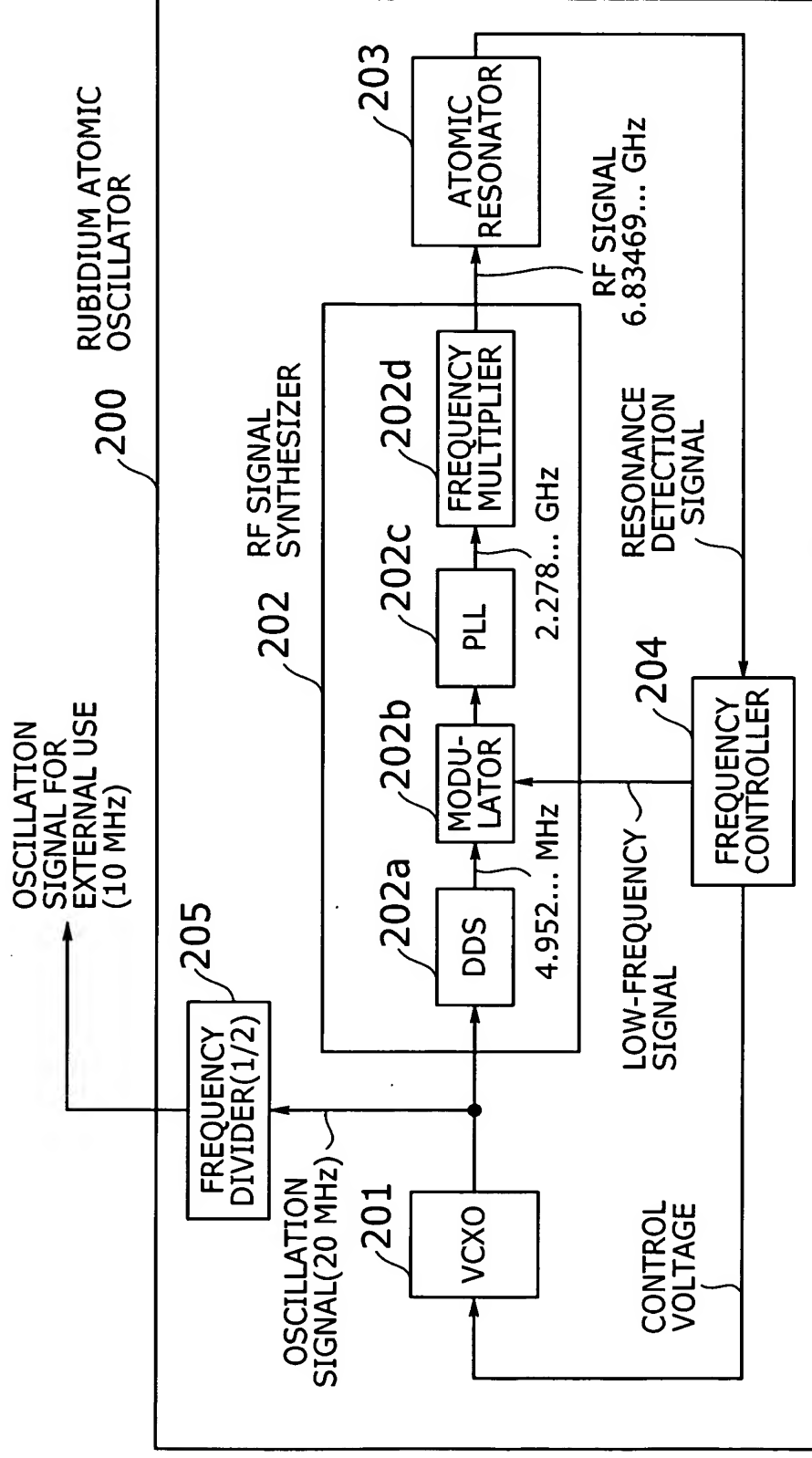


FIG. 19
PRIOR ART